

U.S. PATENT DOCUMENTS+						
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Examiner Initials*	Cita No.		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Pessages or Relevant Figures Appear	
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	FOREIGN PATENT DOCUMENTS								
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Substitute for form 1449B/PTO Complete if Known Application Number 10/723,592 **INFORMATION DISCLOSURE** November 26, 2003 Filing Date STATEMENT BY APPLICANT Augustus K. Uht First Named Inventor 2631 Art Unit (use as many sheets as necessary) Examiner Name Phuong M. Phu 022193-010111US Attorney Docket Number

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Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. *AMD Power Now™ Technology,* product information Advanced Micro Device Sunnyvale, CA USA (2002).	T²
	"AMD Power Now™ Technology," product information Advanced Micro Device Sunnyvale, CA USA (2002).	
2		
-	"Mobile Intel® Pentium® III Processors Intel SpeedStep® Technology," product information available from http://www.intel.com, Intel Corporation Santa Clara, CA USA (2004).	
3	AUSTIN et al. "Making Typical Silicon Matter with Razor", IEEE Computer pp. 57-65 March 2004 (2004).	
4	BURD et al. "A Dynamic Voltage Scaled Microprocessor System," IEEE Journal of Solid-State Circuits 35:1571-1580 (2000).	
5	GINOSAR "Adaptive Synchronization" proceedings of the IEEE International Conference on Computer Design (ICCD), Oct. 1998 (1988).	
6	KURODA et al "Variable Supply-Voltage Scheme forLow-Power High-Speed CMOS Digital Design," IEEE Journal of Solid-State Circuits 33:454-462 (1998).	
7	MERCHANT et al. "Analysis of a control mechanism for a variable speed processor," IEEE Transactions on Computers 45:793-801 (1996).	
8	OLIVIERI "A Low-Power Microcontroller with on-Chip Self-Tuning Digital Clock-Generator for Variable-Load Applications," proceedings of the IEEE International Conference on Computer Design October 10 - 13, 1999 Austin, Texas (1999).	
9	SJOGREN et al. "Interfacing synchronous and asynchronous modules within a high-speed pipeline," IEEE Transactions on VLSI Systems 8:573-583 (2000).	
10	Suzuki "Low Power Adder with Adaptive Supply Voltage," IEEE 21st International Conference on Computer Design October 13 - 15, 2003 San Jose, California (2003).	
11	TZARTZANIS et al. "A 34Word x 64b 10R/6W Write-Through Self-Timed Dual-Supply Voltage Register File," Proceedings of the 2002 IEEE International Solid State Circuits Conference (2002).	
	4 5 6 7 8 9	BURD et al. "A Dynamic Voltage Scaled Microprocessor System," IEEE Journal of Solid-State Circuits 35:1571-1580 (2000). GINOSAR "Adaptive Synchronization" proceedings of the IEEE International Conference on Computer Design (ICCD), Oct. 1998 (1988). KURODA et al "Variable Supply-Voltage Scheme forLow-Power High-Speed CMOS Digital Design," IEEE Journal of Solid-State Circuits 33:454-462 (1998). MERCHANT et al. "Analysis of a control mechanism for a variable speed processor," IEEE Transactions on Computers 45:793-801 (1996). OLIVIERI "A Low-Power Microcontroller with on-Chip Self-Tuning Digital Clock-Generator for Variable-Load Applications," proceedings of the IEEE International Conference on Computer Design October 10 - 13, 1999 Austin, Texas (1999). SJOGREN et al. "Interfacing synchronous and asynchronous modules within a high-speed pipeline," IEEE Transactions on VLSI Systems 8:573-583 (2000). Suzuki "Low Power Adder with Adaptive Supply Voltage," IEEE 21st International Conference on Computer Design October 13 - 15, 2003 San Jose, California (2003).

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